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GAFE

GLAST ACD Front End Electronics ASIC

Charge Splitting: A Test Report

Design Version Proto 1-1 (GAFE1)

Oct 1, 2002

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Scope:

The scope and intent of this document is to describe the test results to verify the Charge Splitting in the GLAST ACD ASIC (GAFE) for the Front End Electronics. Linearity tests were done with GAFE1, the prototype version which has the same analog section as GAFE2. However, GAFE2 which has additional DACs, has weak buffers which limited the testing that could be done, so only minimal testing was done with GAFE2.

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1. Introduction:

This Document describes only the tests pertaining to the Charge Splitting of the GLAST ACD front end electronics ASIC GAFE. The test results of the various other parameters of the ASIC have been reported in another test report.

2. GAFE description

The GAFE ASIC is the front-end analog interface to the PMTs providing signal conditioning of the ionizing event signals for subsequent digitization and processing. The GAFE ASIC provides amplification, shaping, discrimination and timing functions for signal processing by the ACD. The GAFE ASIC is described in more detail in another document that describes the ASIC requirements and architecture.

In the normal mode of operation, the signal from the PMT is terminated in a 33 Pf capacitor, the charge initially stored across this capacitor is then bled off by two resistors which go to the inputs of two low impedance amplifiers. The ratio of these two resistors determine the amount of charge splitting, or the relative gain of the two channels. In the high gain channel, the input resistance is 12K, and for the low gain channel, the input resistance is 1.2Meg ohm, thus establishing a theoretical gain ratio of 1: 100. In the following tests, the value of the resistances were decreased, and the capacitance value increased to maintain the same RC time constant. The results are reported below.

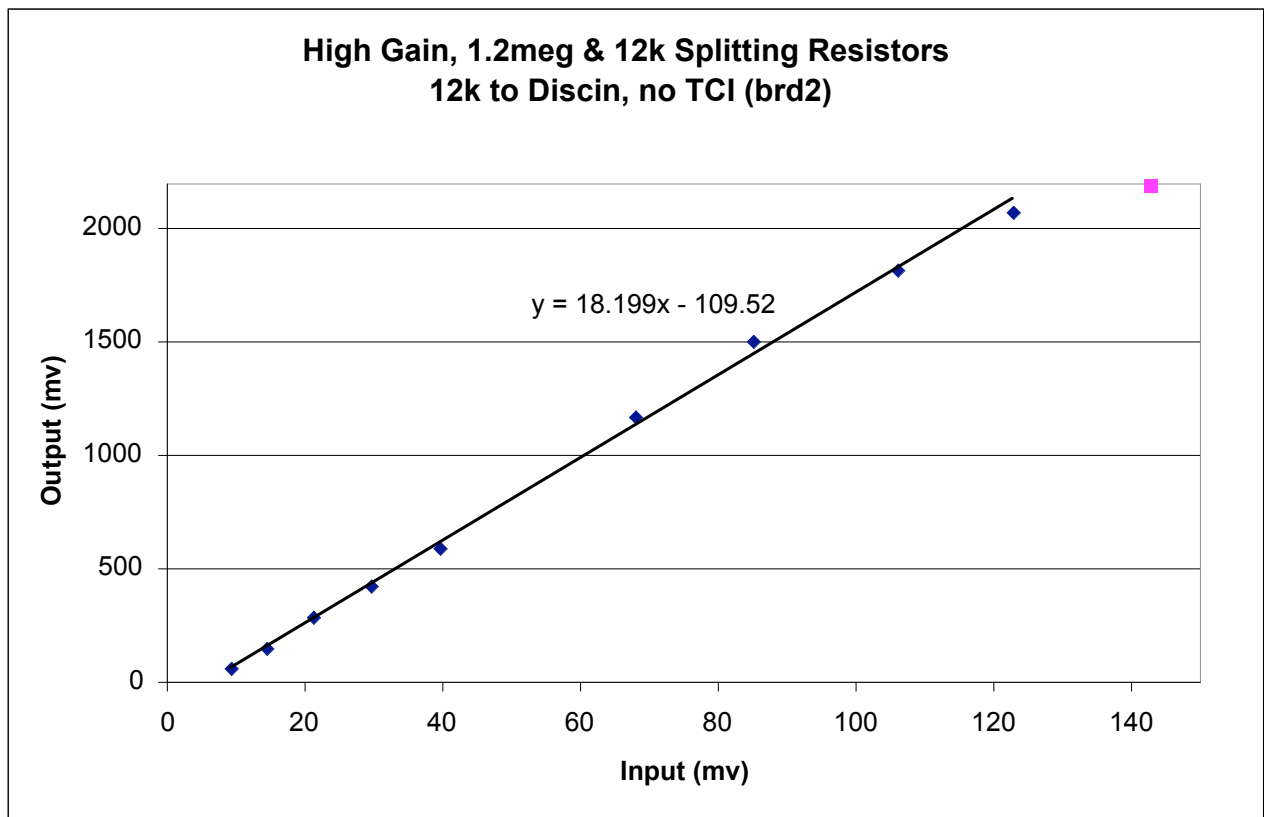
3. Test Results

3.1 12k, 1.2 Meg Ohm, and 120K to discin, Testing with PMT and LED:

The PMT used was, part # ZL0609, R4443 Q-2, with a gain of 6.2 as measured by Alex Moiseev. The PMT was stimulated with a red LED with a pulse of 170 ns width, and the amplitude of the pulse to the led was varied to stimulate the PMT up to 1000 MIPs approximately. For the tests reported below, the output of the PMT was connected through approximately 10 inch cable length to the node common to the two charge splitting resistors. The charge splitting resistors that were used were 12 to the "salo" input and 1.2 Meg to the "sahi" input. The input capacitance of 33pf was not used as the cable capacitance was estimated to be even a little more than that. In addition a 10x scope probe with a capacitance of 10.8Pf was connected to the input to measure the PMT output. Since the PMT output has statistical fluctuations, averaging of the waveforms was used on the scope.

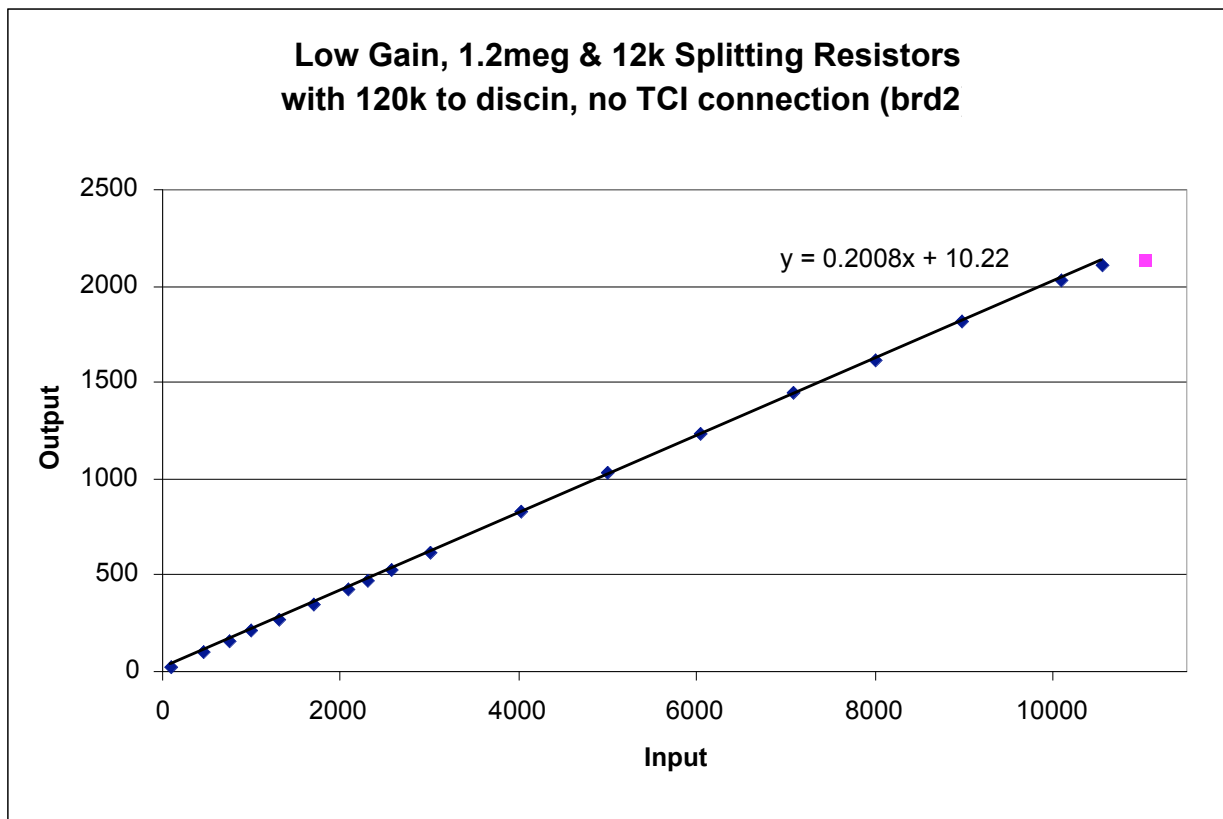
The measurements for the high gain channel are shown below. The resistances used were 12 to the salo input, 1.2Meg to the sahi input, 12k to the discin input, and the test charge injection pad, tci, was left unconnected.

PMT Out (mv)	High Gain (mv)
143	2193
123	2070
106	1820
85	1507
68	1166
39.57	591
29.76	422
21.4	282
14.6	143
9.5	55



The measurements for the Low gain channel are shown below. The resistances used were 12 to the salo input, 1.2Meg to the sahi input, 120k to the discin input, and the test charge injection pad, tci, was left unconnected.

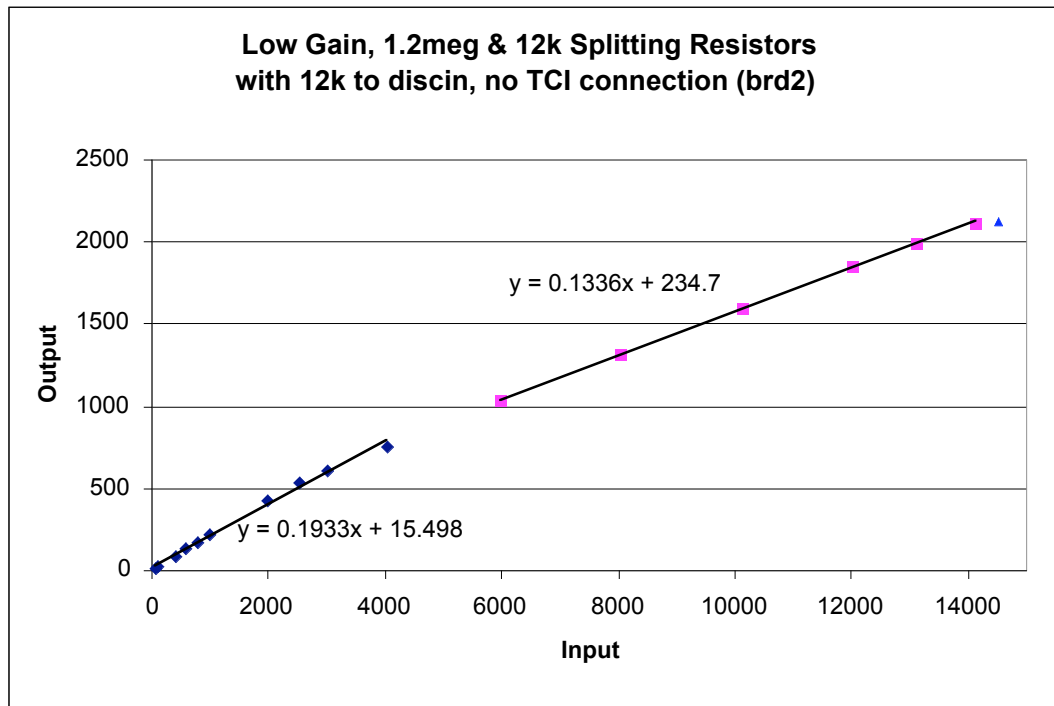
PMT Out (mv)	SA low gain (mv)
11033	2127
10565	2112
10093	2032
8988	1817
7995	1615
7085	1445
6050	1237
5008	1027
4032	830
3005	619
2560	529
2309	475
2085	429
1700	347
1320	273
1002	208
762	158
470	98.9
99.3	20.72



3.2 12k, 1.2 Meg Ohm, and 12K to discin, Testing with PMT and LED:

PMT Out (mv)	SA low gain (mv)
14519	2126
14145	2117
13106	1994
12032	1845
10131	1588
8051	1310
5987	1034
4026	757
3020	609
2520	530
1980	422
1000	216
797	170
595	128.5
400	88
111	25.25
62	14.18

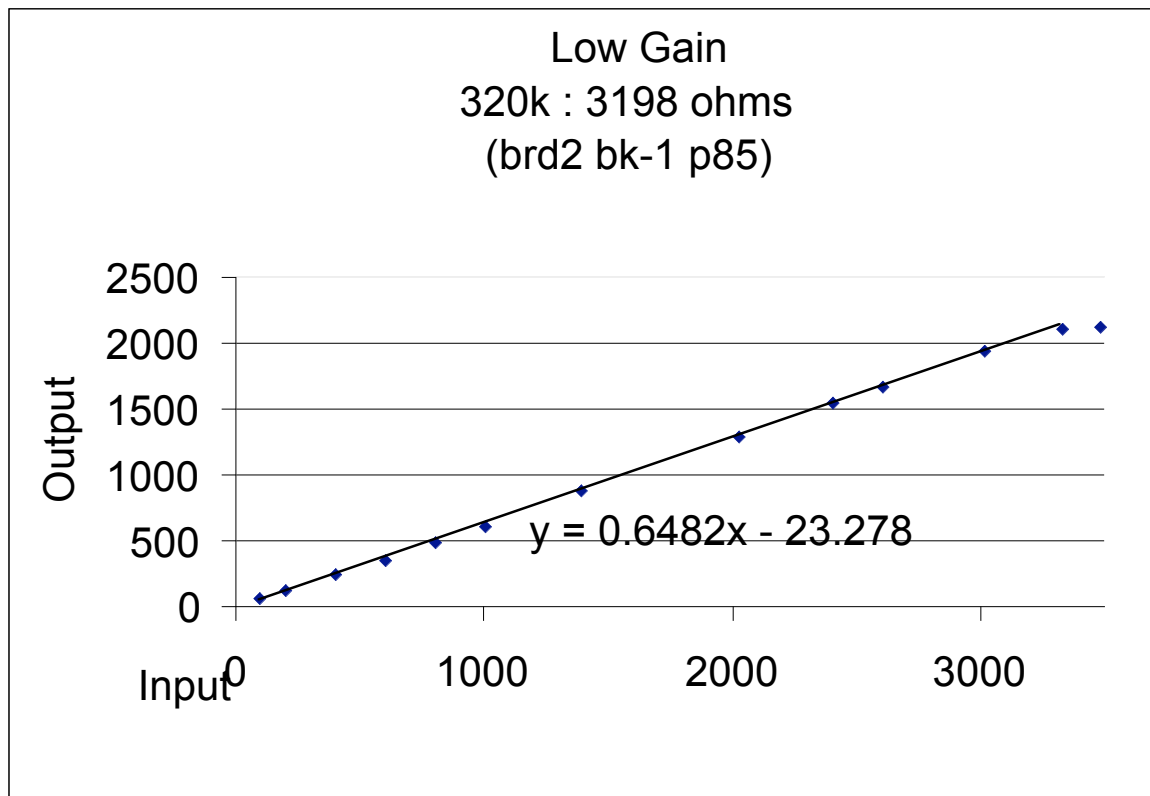
When the resistance to the discriminator input, discin, is reduced from 120k to 12k, the effect of protection pads on the linearity is visible as shown in the measurements below. The pads on the ASICs have protection diodes which clamp the signal to the ground and supply if the input signal were to exceed these voltage limits. For large signals, these diodes kick in and affect the linearity. For the pad to which the "salo", the low energy channel input, this is not a problem as the protection diodes provide additional path to AC ground. However, the pad for the discin, does have an effect on the linearity as the protection diodes provide additional path to the ground for large signals.



3.3 3.2k, 320k Ohm, and 12K to discin, Testing with a Pulser:

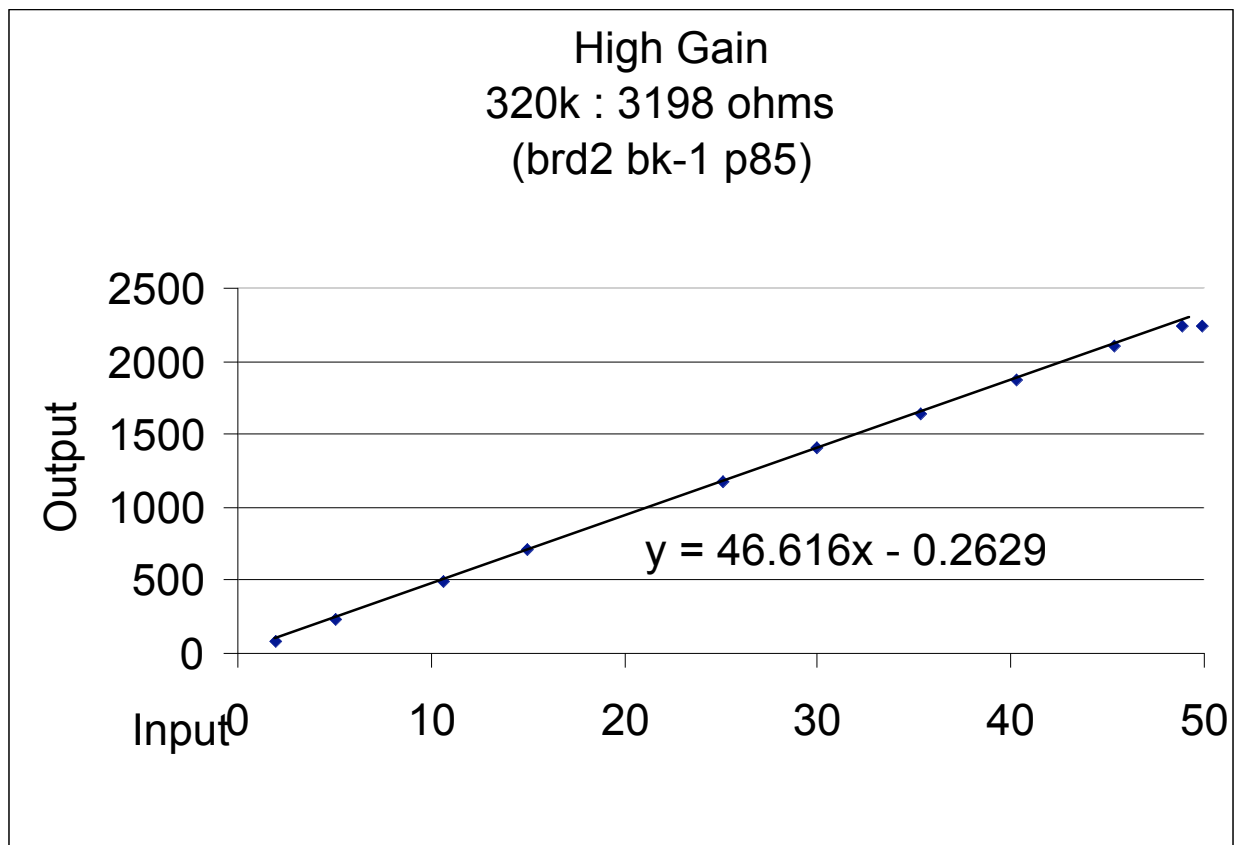
Since the resistances were dropped, the input capacitor was raised from 33pf to 120pf to maintain the same time constant at the input. The charge was injected using a square pulse generator through the capacitor. The results show that even though the 12k to discin is connected, it does not have much impact on linearity as the resistance to the high gain channel is much lower at 3.2K.

Input Pulse (mv)	SA Low gain (mv)
99.12	64
200.9	123.4
405	238.3
605	355
806	480
1002	609
1391	877
2030	1291
2409	1540
2609	1674
3021	1942
3332	2108
3483	2114



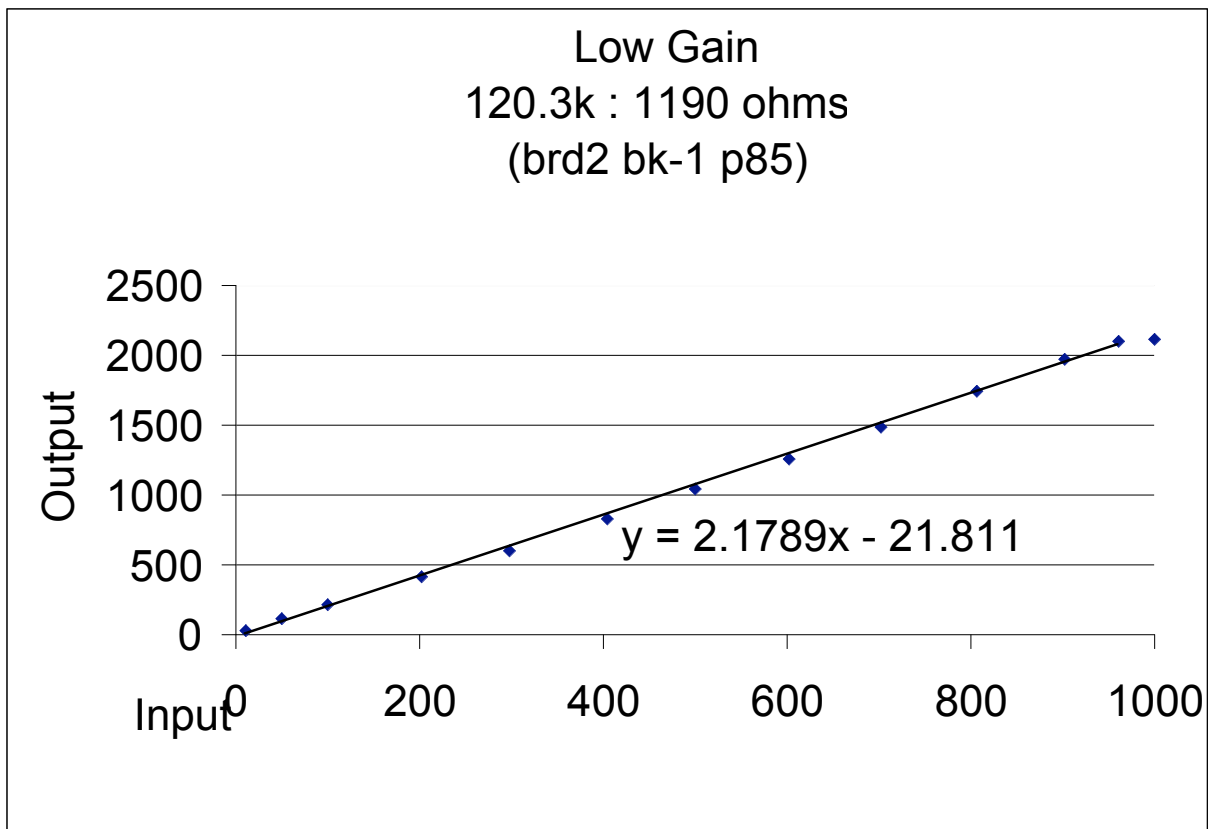
The measurements for the high gain channel are shown below:

Input Pulse (mv)	SA High gain (mv)
1.95	80
5.1	233
10.6	498.6
14.99	707
25.1	1176
30	1406
35.3	1644
40.3	1876
45.3	2103
48.9	2245
49.9	2247

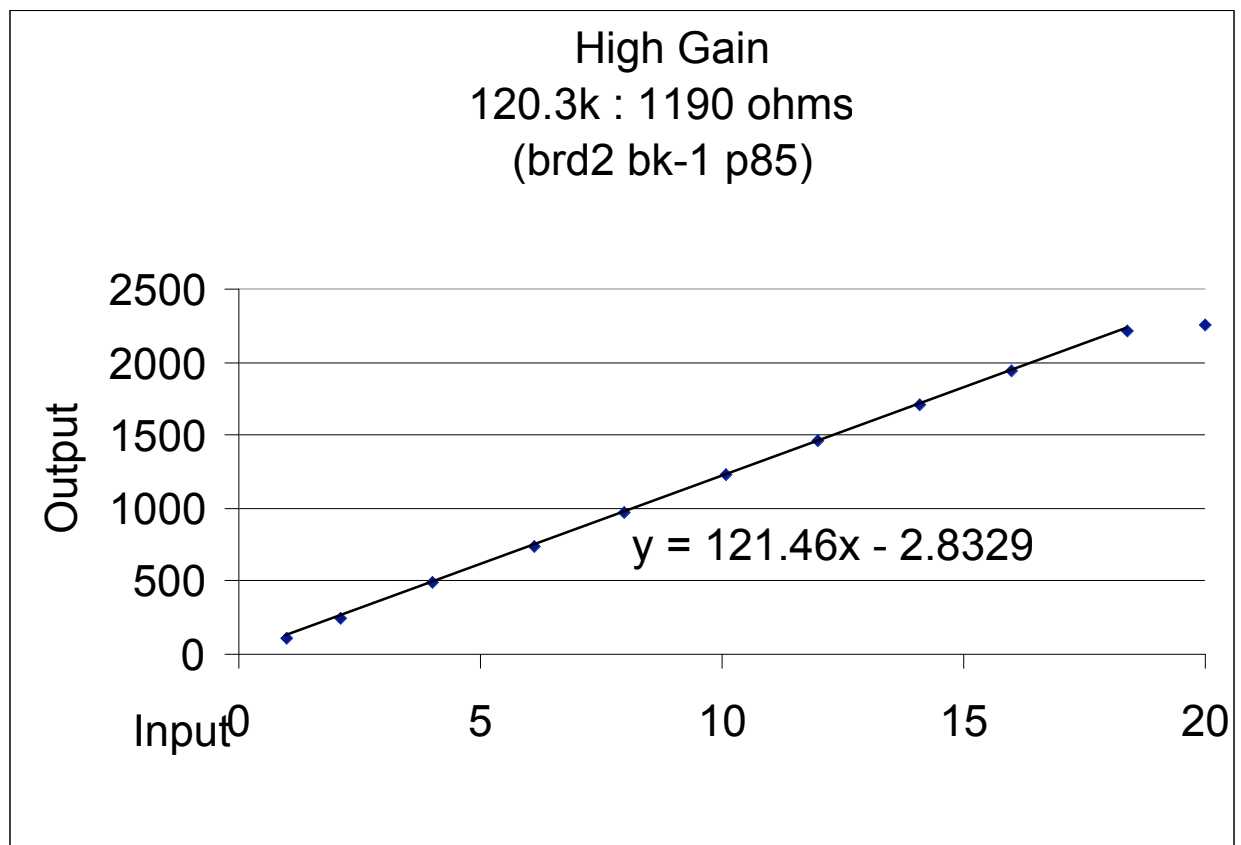


3.4 1.2k, 120k Ohm, and 12K to discin, Testing with a Pulser:

Input Pulse (mv)	SA Low gain (mv)
11.1	28.16
49.8	120
100.1	217.6
202	408
298.5	595.5
404.6	826.5
499	1037
602`	1264
703	1491
807	1741
903	1976
960	2105
1001	2116

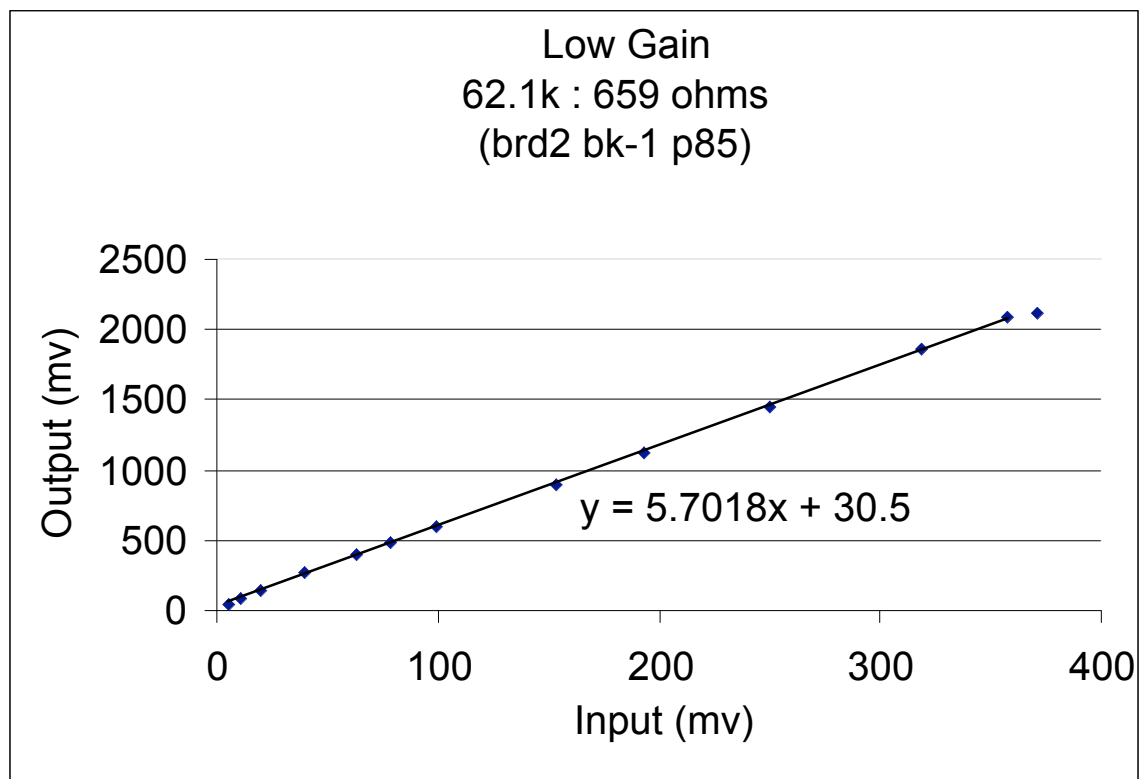


Input Pulse (mv)	SA High gain (mv)
0.98	110.7
2.1	242.5
4	487
6.1	740
7.98	975
10.1	1229
11.98	1457
14.1	1711
15.98	1941
18.4	2219
20	2249

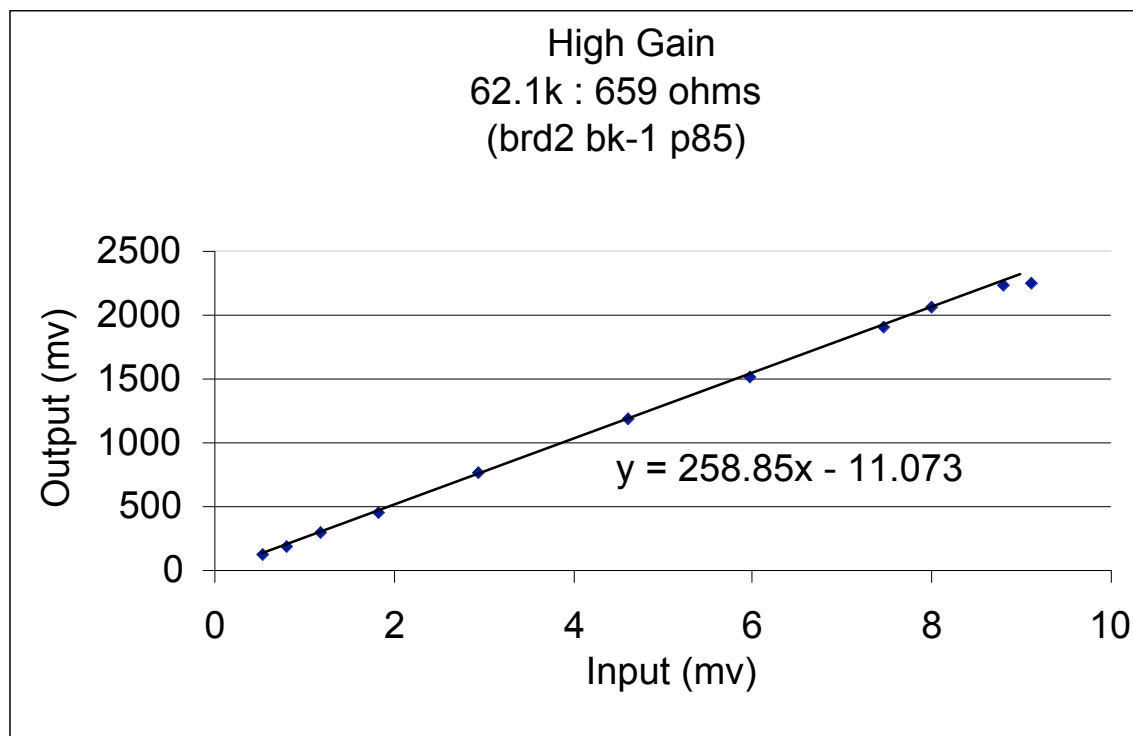


3.5 660 ohm, 62K Ohm, and 12K to discin, Testing with a Pulser:

Input Pulse (mv)	SA Low gain (mv)
5.3	45
11	85.4
19.5	148
39.5	273
62.9	398
79	488
99.1	596.7
153.2	894
193.3	1121
250	1449
318.5	1858
358	2092
371	2121



Input Pulse (mv)	SA High gain (mv)
0.538	124.3
0.795	189.6
1.18	295.3
1.82	460
2.93	758
4.6	1188
5.96	1523
7.47	1913
8	2067
8.8	2237
9.1	2247



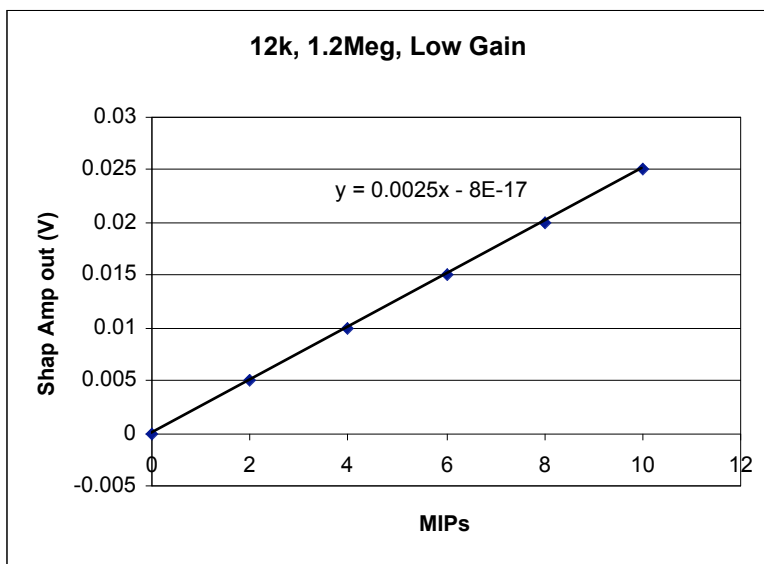
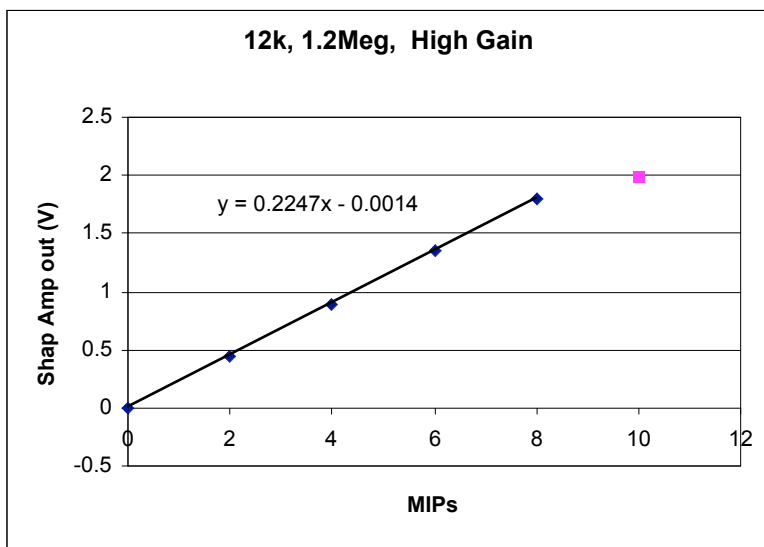
4. Simulations

To check the charge splitting, simulations were done and relative gains of the high and low energy channels computed as shown below.

4.1 12K and 1.2 Meg Ohm, 33Pf : Simulations

Input MIPs SA, LE out (v) SA, HE out (v)

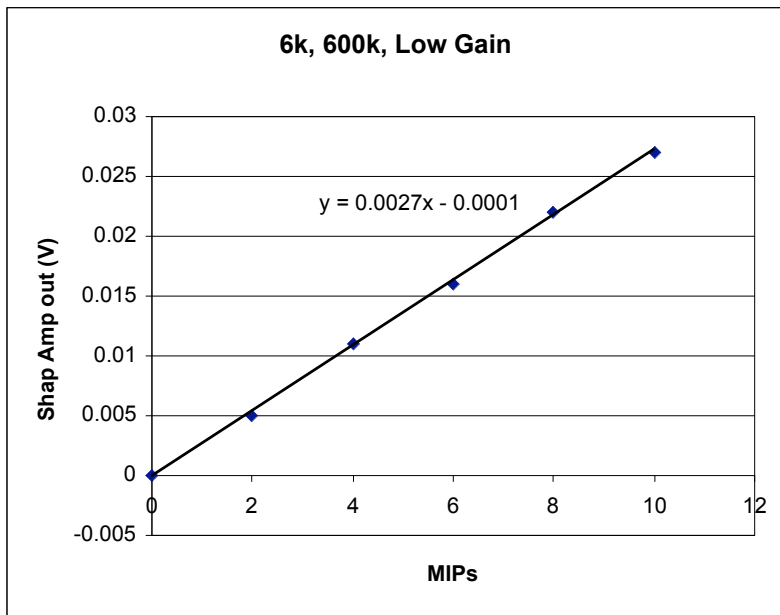
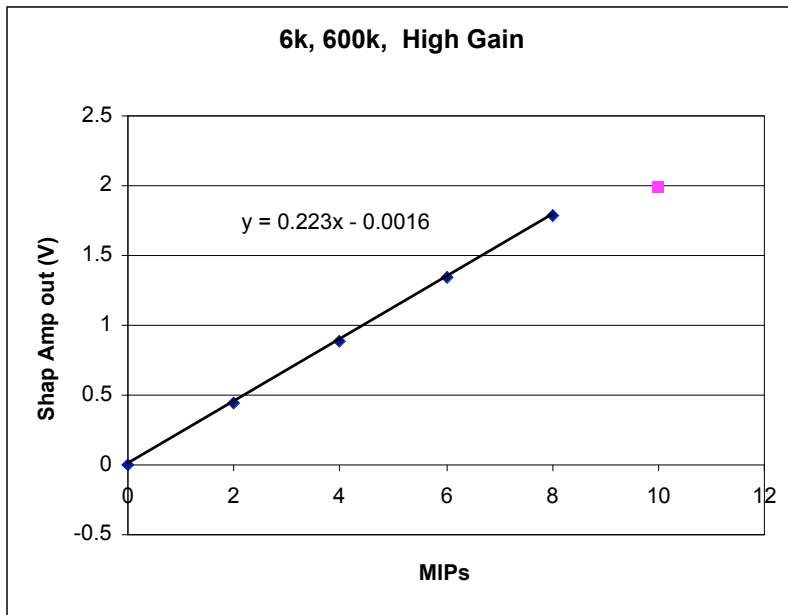
0	0	0
2	0.447	0.005
4	0.896	0.01
6	1.347	0.015
8	1.797	0.02
10	1.982	0.025



4.2 6K and 600K, 68Pf : Simulations

Input MIPs SA, LE out (v) SA, HE out (v)

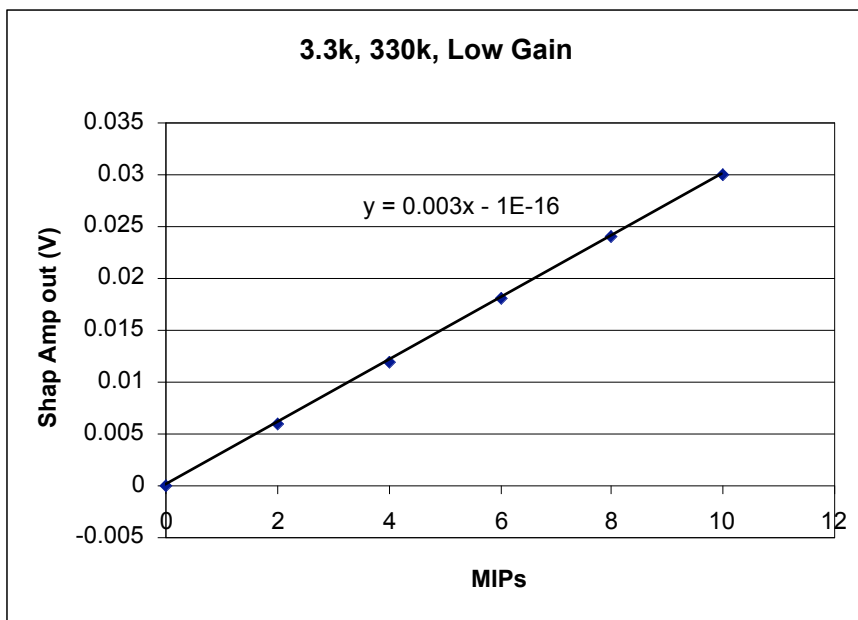
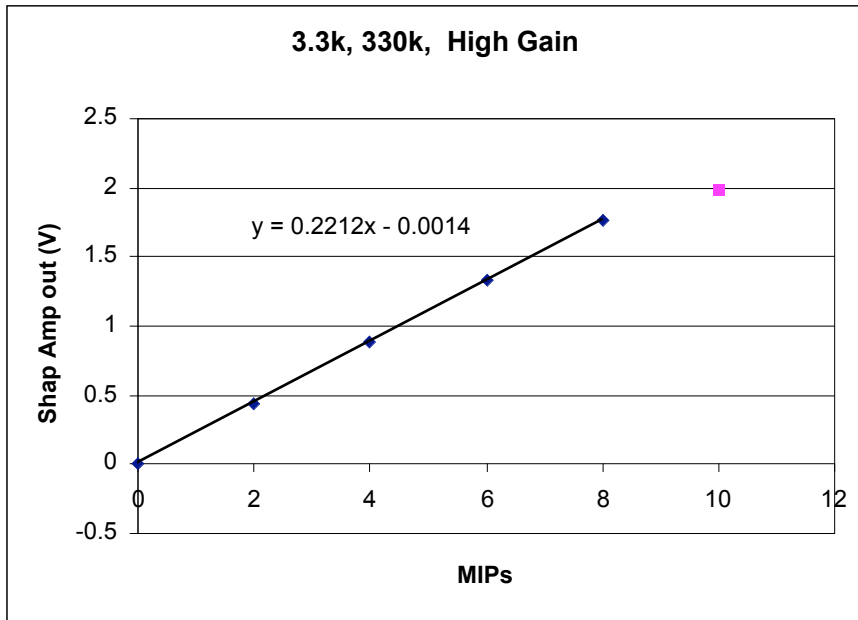
0	0	0
2	0.443	0.005
4	0.889	0.011
6	1.336	0.016
8	1.783	0.022
10	1.982	0.027



4.3

Input MIPs SA, LE out (v) SA, HE out (v)

0	0	0
2	0.44	0.006
4	0.882	0.012
6	1.325	0.018
8	1.769	0.024
10	1.982	0.03



5. Summary:

These tests were done to check the charge splitting performance of the PHA channels, and to check how the charge splitting performance got affected as the input resistances were decreased. The relative gains of the high and low energy channels for the test measurements and simulations are summarized below:

<u>Input Resistances</u>	<u>Relative gain (Tested)</u>	<u>Relative gain (Simulations)</u>
12k, 1.2 Meg Ohm	90.99	90
6k, 600k	-	82.59
3.2k, 320k	71.9	73.66
1.2k, 120k	55.7	-
660, 62k	45.26	-

The comparison of the relative gains of the low and high energy channels for the lower resistance values of 12 k and 3.2k, show agreement between the test measurements and the simulations.

The above table also shows how the relative gain drops as the resistance is decreased. It is seen that for resistance values of 3.2K or less, the gain has dropped to 73.6% or lower.